WHAT IS CLAIMED:

1. A gate structure of a non-volatile integrated circuit memory device comprising:

a thermal oxidation layer on a substrate beneath the gate structure and that defines a side wall of the gate structure;

an oxygen diffusion barrier layer on the side wall of the gate structure; and

a floating gate on the thermal oxidation layer having a curved side wall portion.

2. A gate structure according to Claim 1 wherein at least a lower portion of the curved side wall portion curves away from the side wall of the gate structure toward a surface of the floating gate that faces the substrate.

3. A gate structure according to Claim 2 wherein the surface comprises a first surface, wherein the curved side wall of the floating gate further comprises:

an upper curved side wall portion of the floating gate that curves away from the side wall of the gate structure toward a second surface of the floating gate that faces away from the substrate.

4. A gate structure according to Claim 2 further comprising:

a linear portion of the side wall of the floating gate directly coupled to the curved portion of the side wall at a first point, wherein the first point is spaced apart from an interface between the thermal oxidation layer and the substrate by a first distance; and

wherein a linear portion of the surface that faces the substrate is spaced apart from the interface by a second distance that is less than the first distance.

5. A gate structure according to Claim 4 wherein the surface comprises a first surface, wherein the curved side wall of the floating gate further comprises an upper curved side wall portion of the floating gate that curves away from the side wall of the gate structure toward a second surface of the floating gate that faces away from the substrate, the gate structure further comprising:

a control gate on the floating gate;

an inter-gate dielectric layer between the control gate and the floating gate including a silicon nitride layer, wherein a linear portion of the second face is spaced apart from the silicon nitride layer by a third distance; and

wherein the linear portion of the side wall of the floating gate that is directly coupled to the upper curved side wall portion of the floating gate at a second point that is spaced apart from the silicon nitride layer by a fourth distance that is greater than the third distance.

6. A gate structure according to Claim 5 wherein a difference between the first and second distances is greater than a difference between the third and fourth distances.

7. A gate structure according to Claim 3 wherein a length of the lower curved side wall is greater than a length of the upper curved side wall.

8. A gate structure according to Claim 1 further comprising:

a control gate on the floating gate having a curved side wall.

9. A gate structure according to Claim 8 wherein a length of the curved side wall of the control gate is less than the length of the upper curved side wall.

10. A gate structure according to Claim 1 further comprising:

a control gate on the floating gate; and

an inter-gate dielectric layer between the control gate and the floating gate including a silicon nitride layer having a curved side wall.

11. A gate structure according to Claim 10 wherein the curved side wall of the silicon nitride layer curves away from the side wall of the gate structure toward the floating gate.

12. A method of forming a gate structure of a non-volatile integrated circuit memory device comprising:

forming a gate structure including a floating gate on an oxide layer on a substrate;

forming an oxygen diffusion barrier layer on a side wall of the gate structure above the oxide layer; and

forming a thermal oxidation layer from the oxide layer beneath the floating gate and on the floating gate between the oxygen diffusion barrier layer and the floating gate to define a curved side wall portion of the floating gate.

13. A method according to Claim 12 wherein the step of forming a thermal oxidation layer comprises the step of:

forming an insulating layer on the floating gate and on the substrate beside the gate structure; and

heating the insulating layer and the oxide layer to form the thermal oxidation layer on the substrate beneath the oxygen diffusion barrier layer to provide a pathway in the thermal oxidation layer through the oxygen diffusion barrier layer.

14. A method according to Claim 13 wherein the step of forming a gate structure further comprises:

forming an inter-gate oxide layer on the floating gate; and

forming a silicon nitride layer on the inter-gate oxide layer to form an inter-gate dielectric layer on the floating gate.

15. A method according to Claim 14 wherein the step of forming a thermal oxidation layer further comprising forming the thermal oxidation layer in an atmosphere including oxygen atoms that reach silicon atoms included in the floating gate via the pathway in a first amount.

16. A method according to Claim 15 wherein the step of forming a thermal oxidation layer further comprising forming the thermal oxidation layer in the atmosphere including oxygen atoms that reach silicon atoms included in the inter-gate dielectric layer via the pathway in a second amount that is less than the first amount.

17. A method according to Claim 16 further comprising:

forming a control gate on the inter-gate dielectric layer, wherein the step of forming a thermal oxidation layer further comprising forming the thermal oxidation

layer in the atmosphere including oxygen atoms that reach silicon atoms included in the control gate via the pathway in a third amount that is less than the second amount.

18. A method according to Claim 12 wherein at least a lower portion of the curved side wall portion curves away from the side wall of the gate structure toward a surface of the floating gate that faces the substrate.

19. A method according to Claim 18 wherein the surface comprises a first surface, wherein the curved side wall of the floating gate further comprises:

an upper curved side wall portion of the floating gate that curves away from the side wall of the gate structure toward a second surface of the floating gate that faces away from the substrate.

20. A method according to Claim 18 further comprising:

a linear portion of the side wall of the floating gate directly coupled to the curved portion of the side wall at a first point, wherein the first point is spaced apart from an interface between the thermal oxidation layer and the substrate by a first distance; and

wherein a linear portion of the surface that faces the substrate is spaced apart from the interface by a second distance that is less than the first distance.

21. A method according to Claim 19 wherein a length of the lower curved side wall is greater than a length of the upper curved side wall.

22. A method according to Claim 12 further comprising:

forming a control gate on the floating gate having a curved side wall.

23. A method according to Claim 22 wherein a length of the curved side wall of the control gate is less than the length of the upper curved side wall.

24. A method according to Claim 12 further comprising:

forming a control gate on the floating gate; and

forming an inter-gate dielectric layer between the control gate and the floating gate including a silicon nitride layer having a curved side wall.

25. A method for fabricating a transistor of a nonvolatile memory device, comprising:

forming a gate pattern on an integrated circuit substrate, the gate pattern including a gate oxide layer, a floating gate, an inter-gate dielectric pattern, and a control gate which are stacked in the order named;

forming a diffusion barrier layer on an entire surface of an integrated circuit substrate including the gate pattern;

anisotropically etching the diffusion barrier layer to form a diffusion barrier spacer over a lateral side of the gate pattern; and

thermally oxidizing an integrated circuit substrate including the diffusion barrier spacer.

26. The method as set forth in Claim 25, characterized in that the inter-gate dielectric pattern is made of silicon oxide, silicon nitride, and silicon oxide which are stacked in the order named.

27. The method as set forth in Claim 25, characterized in that the formation of the gate pattern comprises:

forming a device isolation layer at a predetermined region of the integrated circuit substrate to define an active region;

forming a gate oxide layer on the active region;

forming a lower conductive pattern on the gate oxide layer, the lower conductive pattern being disposed in parallel with the active region;

forming an inter-gate dielectric and an upper conductive layer on an entire surface of an integrated circuit substrate including the lower conductive pattern; and

successively patterning the upper conductive layer, the inter-gate dielectric, and the lower conductive pattern, the patterning being vertical to the active region.

28. The method as set forth in Claim 27, characterized in that the gate oxide layer is a silicon oxide layer which is formed by thermally oxidizing the active region.

29. The method as set forth in Claim 27, characterized in that the lower conductive pattern is made of polysilicon.

30. The method as set forth in Claim 27, characterized in that the upper conductive layer is made of polysilicon and silicide which are stacked in the order named.

31. The method as set forth in Claim 27, before patterning the upper conductive layer, further comprising forming a capping layer on the upper conductive layer.

32. The method as set forth in Claim 25, characterized in that the diffusion barrier layer is a silicon nitride layer which is formed by means of chemical vapor deposition (CVD).

33. The method as set forth in Claim 25, before forming the diffusion barrier layer, further comprising forming a buffer insulation layer to cover an entire surface of an integrated circuit substrate including the gate pattern.

34. The method as set forth in Claim 33, characterized in that the buffer insulation layer is a silicon nitride layer which is formed by means of CVD.

35. The method as set forth in Claim 25, characterized in that the thermal oxidation is performed for a lower edge of the floating gate.